



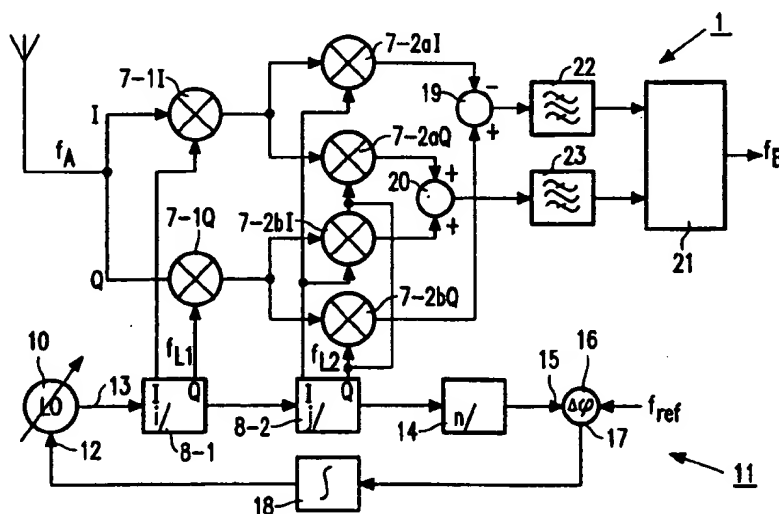
PCT

WORLD INTELLECTUAL PROPERTY ORGANIZATION  
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification <sup>6</sup> : H03L 7/08	A2	(11) International Publication Number: WO 98/40968 (43) International Publication Date: 17 September 1998 (17.09.98)
(21) International Application Number: PCT/IB98/00238 (22) International Filing Date: 27 February 1998 (27.02.98) (30) Priority Data: 97200739.7 12 March 1997 (12.03.97) EP (34) Countries for which the regional or international application was filed: NL et al. (71) Applicant: KONINKLIJKE PHILIPS ELECTRONICS N.V. [NL/NL]; Groenewoudseweg 1, NL-5621 BA Eindhoven (NL). (71) Applicant (for SE only): PHILIPS NORDEN AB [SE/SE]; Kottbygatan 7, Kista, S-164 85 Stockholm (SE). (72) Inventor: BALTUS, Petrus, Gerardus; Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL). (74) Agent: MAK, Theodorus, N.; Internationaal Octrooibureau B.V., P.O. Box 220, NL-5600 AE Eindhoven (NL).		(81) Designated States: JP, European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).  Published Without international search report and to be republished upon receipt of that report.

(54) Title: A FREQUENCY CONVERSION CIRCUIT



(57) Abstract

In a frequency-conversion circuit having a multistage frequency-converting means, at least two stages are coupled through divider means to one and the same voltage-controlled oscillator. Inputs of the multistage frequency-converting means are coupled to one another in a phase error-free manner by frequency divider means embodied as easy-to-implement counters. By virtue thereof, one phase locked loop including such a voltage-controlled oscillator can be dispensed with, thus saving surface area, components on a chip and reducing costs and weight, which is particularly important in connection with the application of the frequency-conversion circuit in mobile communication equipment.

**FOR THE PURPOSES OF INFORMATION ONLY**

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AL	Albania	ES	Spain	LS	Lesotho	SI	Slovenia
AM	Armenia	FI	Finland	LT	Lithuania	SK	Slovakia
AT	Austria	FR	France	LU	Luxembourg	SN	Senegal
AU	Australia	GA	Gabon	LV	Latvia	SZ	Swaziland
AZ	Azerbaijan	GB	United Kingdom	MC	Monaco	TD	Chad
BA	Bosnia and Herzegovina	GE	Georgia	MD	Republic of Moldova	TG	Togo
BB	Barbados	GH	Ghana	MG	Madagascar	TJ	Tajikistan
BE	Belgium	GN	Guinea	MK	The former Yugoslav Republic of Macedonia	TM	Turkmenistan
BF	Burkina Faso	GR	Greece	ML	Mali	TR	Turkey
BG	Bulgaria	HU	Hungary	MN	Mongolia	TT	Trinidad and Tobago
BJ	Benin	IE	Ireland	MR	Mauritania	UA	Ukraine
BR	Brazil	IL	Israel	MW	Malawi	UG	Uganda
BY	Belarus	IS	Iceland	MX	Mexico	US	United States of America
CA	Canada	IT	Italy	NE	Niger	UZ	Uzbekistan
CF	Central African Republic	JP	Japan	NL	Netherlands	VN	Viet Nam
CG	Congo	KE	Kenya	NO	Norway	YU	Yugoslavia
CH	Switzerland	KG	Kyrgyzstan	NZ	New Zealand	ZW	Zimbabwe
CI	Côte d'Ivoire	KP	Democratic People's Republic of Korea	PL	Poland		
CM	Cameroon	KR	Republic of Korea	PT	Portugal		
CN	China	KZ	Kazakhstan	RO	Romania		
CU	Cuba	LC	Saint Lucia	RU	Russian Federation		
CZ	Czech Republic	LI	Liechtenstein	SD	Sudan		
DE	Germany	LK	Sri Lanka	SE	Sweden		
DK	Denmark	LR	Liberia	SG	Singapore		
EE	Estonia						

## A FREQUENCY CONVERSION CIRCUIT

The present invention relates to a frequency-conversion circuit comprising a multistage frequency-converting means and an oscillator output coupled to at least one oscillator input of the multistage frequency-converting means.

The present invention also relates to a telecommunication system, a receiver, a transmitter, a transceiver, an integrated circuit, and a telephone device provided with such a frequency-conversion circuit.

Such a frequency-conversion circuit is known from "High Integration CMOS RF Transceivers", Proc. of the Workshop on Advances in Analog Circuit Design, April 2-3-4, 1996, Lausanne-Ouchy, Switzerland, by F. Brianti et al., 14 pages. This article describes in particular integrated digital radio architectures having a frequency up or down converting means usable, for example, in low-IF, such as zero-IF, or wideband-IF configurations. By definition, a low-IF configuration, such as a receiver, transmitter or transceiver, is a configuration, wherein the intermediate frequency (IF) is close to zero, or zero in the case of zero-IF. Some known advantages of zero-IF configurations are the high degree of integration on a chip that can be achieved as compared to a heterodyne or conventional IF configuration, because of the possibility to apply filters, such as low-pass filters for channel selectivity, that can be integrated at low cost. Reduced power dissipation, fewer interference problems and better crosstalk control than in a conventional configuration that requires external components can be achieved with a careful design using this zero-IF architecture. The frequency conversion is implemented by means of two stages of mixers (see figure 2) resulting in a multistage frequency conversion in order to reduce the requirements imposed upon image rejection filters in front of the mixers as compared to conventional architectures. The mixer stages are quadrature mixer stages each having an I-path and a Q-path in order to properly distinguish between positive and negative frequencies, corresponding to upper and lower sidebands of an input RF signal. These quadrature mixers eliminate an off-chip IF filter function. Each of the two stages is being fed by a separate voltage-controlled oscillator (VCO) phase-locked loop (PLL) synthesizer circuit. Both

synthesizer circuits are connected to a common crystal oscillator. The problem of the known frequency conversion circuit is that two synthesizer circuits are needed, which circuits lead to significant costs and require a large surface, area and much power.

5

It is an object of the present invention to reduce the chip area and power consumption needed for integrated architectures. To achieve this, the frequency-conversion circuit according to the invention is characterised in that the frequency-conversion circuit comprises a frequency-divider means coupled between the oscillator output and at least one  
10 further oscillator input of the multistage frequency-converting means. The frequency-conversion circuit according to the invention has the advantage that one VCO/PLL circuit can be dispensed with, thus saving components, cost and chip area, and reducing power dissipation and weight, which is particularly important in mobile communication applications of the frequency-conversion circuit, such as telephone systems. In addition, integration of  
15 only one of such VCO/PLL circuit is more easy and only involves a minimum number of components.

In an embodiment of the frequency-conversion circuit according to the invention, the frequency divider means comprises a counter means. Such counter means are very simple to integrate. Furthermore, the counter means provide for an exact relation as a  
20 function of time, in particular the phase, between the respective oscillator signals intended for each stage of the multistage frequency-converting means. Because of the inherent phase accuracy between the respective oscillator signals derived from both respective outputs of the counter means, a good image or mirror signal suppression is automatically achieved so that, if necessary at all, a modest image rejection-suppression filter will be sufficient in practise to  
25 reveal a high-quality frequency conversion. In general, the counter means already have or can easily be provided with outputs for providing both the I and Q oscillator signals to be applied to the I and Q paths respectively, of the multistage frequency-converting means. So separate 90° phase shifters are no longer necessary in the coupling or direct connection between the generally local oscillator and, in particular, the Q paths' oscillator inputs of the  
30 multistage frequency-converting means.

These and other aspects and advantages of the present invention will be apparent from and further elucidated with reference to the embodiments and figures described

hereinafter. Similar elements in the separate figures are provided with the same reference numerals. In the drawing:

Fig. 1 shows a principle scheme of one embodiment of the frequency-conversion circuit according to the present invention;

5 Fig. 2 shows an elaborate worked out embodiment of one stage of a multistage frequency-converting means, and a second stage thereof for application in the frequency-conversion circuit of figure 1;

Fig. 3 shows another embodiment of the frequency-conversion circuit according to the invention;

10 Fig. 4 shows a frequency divider means comprising a series arrangement of counters for application in the frequency-conversion circuit according to the invention;

Fig. 5 shows a frequency divider means comprising a parallel arrangement of counters for application in the frequency-conversion circuit according to the invention;

15 Fig. 6 shows a frequency divided by 3 means for application in the frequency divider means of figures 4 or 5; and

Fig. 7 schematically shows a telecommunication system comprising transmitters and/or receivers having one or more frequency-conversion circuits according to the invention.

20

Figure 1 shows a frequency-conversion circuit 1 that can be used in a telecommunication system 2 as schematically shown in figure 7. The telecommunication system 2 shown comprises one or more receivers 3, transmitters 4, and/or transceivers  
25 (=transmitter/receiver) 5, each of which contains apart from other circuits, the frequency-conversion circuit 1. The telecommunication system can be a transmission system, such as a radio transmission system, a cordless or cellular telephone system or the like, an audio- or video system, a control system, a telemetry system, a local area network, a wide area network etcetera. Such a frequency-conversion circuit 1 can be used for frequency up  
30 conversion or frequency down conversion dependent on the application in a transmitter 4 or receiver 3, respectively.

For the sake of simplification of the description, figures 1-3 relate to frequency-conversion circuits 1 used in a receiver 3, although the frequency-conversion circuits 1 could equally well be used in a transmitter 4 or transceiver 5.

The frequency-conversion circuit 1 comprises an antenna 6 connected to a multistage frequency-converting means 7 showing two conversion stages or mixing stages 7-1 and 7-2 having oscillator inputs referred to in this figure as  $f_{L1}$  and  $f_{L2}$ . The multistage frequency-converting means 7 could include more than two stages although nowadays this is quite uncommon. The antenna signal  $f_A$  is mixed in stage 7-1 with a first local oscillator signal  $f_{L1}$  and the resulting mixed signal is then mixed in stage 7-2 with a second local oscillator signal  $f_{L2}$  to reveal a baseband signal  $f_B$  after demodulation (not shown in figures 1 and 2). For zero-IF  $f_A = f_{L1} + f_{L2}$ .

In figure 2, the stage 7-1 shows in greater detail a quadrature down conversion in an I-path and a Q-path. The I- and Q paths comprise a mixer 7-1I and 7-1Q, respectively, where to I and Q local oscillator signals  $f_{L1}$  are applied from a frequency divider means 8-1 to be described hereafter. Appropriate  $90^\circ$  phase shifters are provided, as indicated, and the I and Q path signals are subtracted from each other in adder 9 to reveal an intermediate signal to be mixed in stage 7-2 with the second local oscillator signal  $f_{L2}$  provided by a frequency divider means 8-2, to be described hereafter, resulting in the baseband signal  $f_B$ . A local oscillator 10 is coupled to inputs of the multistage frequency converting means 7-1 and 7-2, respectively, as shown in figure 3, that is to say connected through the series arrangement of both frequency divider means 8-1 and 8-2, or as shown in figure 2, connected through the parallel arrangement of both frequency divider means 8-1 and 8-2.

Figure 3 shows a detailed embodiment of how the frequency divider means 8-1, 8-2 are included in only one phase-locked loop 11. The phase-locked loop 11 further comprises the local oscillator in the form of a generally tunable voltage-controlled oscillator 10 having a control input 12 and an oscillator output 13 coupled to the frequency divider means 8-1, which is connected in series to the frequency divider means 8-2 and a further divider 14, which is connected to an input 15 of a phase discriminator 16. The phase discriminator 16 has a reference frequency input for inputting a reference signal  $f_{REF}$ , such as a signal from a conventional crystal oscillator (not shown) and an output 17 coupled to the control input 12 of the voltage controlled oscillator 10 through a loop filter 18 for a stable control of the PLL. The further divider 14 has a divisor that, in dependence on the divisor of the frequency divider means, matches the local oscillator frequency to the frequency of  $f_{REF}$ . In the case shown here, the frequency divider means comprises counter means 8-1, 8-2. These counter means easily provide the I and Q oscillator signals for both  $f_{L1}$  and  $f_{L2}$  signals. Embodiments thereof will be presented in figures 4-6.

Figure 3 further shows details of mixing stage 7-2, which is divided in a first pair of branches, which are connected to mixer 7-1I and which comprise mixers 7-2aI and 7-2aQ, which are connected with minus and plus signs to adders 19 and 20, respectively, and in a second pair of branches, connected to mixer 7-1Q and which comprise mixers 7-2bI and 7-2bQ, which are connected both with plus signs to the adders 19 and 20, respectively. Quadrature output signals of the adders 19 and 20 are led to a demodulator 21 through bandpass filters 22 and 23, respectively, revealing the actual baseband signal  $f_B$ . For zero-IF, these filters 22 and 23 can be embodied as low-pass filters.

The operation of the frequency- conversion circuit 1 of figure 3 will now be described for the case wherein the counter means 8-1, 8-2 are simple binary counters which divide the input-signal frequency by 2. Assuming  $f_A = 900$  MHz, a local oscillator frequency of 1200 MHz, will lead to a value of  $f_{L1} = 1200/2 = 600$  MHz. Consequently,  $f_{L2} = 600/2 = 300$  MHz and the output signal after the second stage 7-2 will lie in the baseband. Tuning can be achieved by stepping of the local oscillator 10 at 4/3 times the channel spacing steps. Moreover, because in this example the local oscillator frequency does not coincide with the RF-antenna frequency, also crosstalk problems are significantly reduced. In addition, an excellent image suppression is achieved in a way which is easy to integrate on a chip, and which does not require external components or, in the case of zero-IF, filters that are very difficult or impossible to integrate, such as polyphase filters, multimixer filters, sequence asymmetric filters and the like.

If, in general, in the series arrangement of counters, the first counter means 8-1 has divisor  $i$  and the second counter means 8-2 has divisor  $j$ , then the equation for zero-IF is:

$$f_{LO} = f_A \cdot i \cdot j / (j + 1)$$

Figure 4 shows a simple way of connecting two 2-counters 8-1 and 8-2 that will generally be included in a phase-locked loop as shown in figure 3. By virtue thereof, an easily integratable fixed phase relation between the I- and Q-outputs is achieved, which reduces problems that emanate from a varying phase. Figure 5 shows an embodiment of counters 24 and 25 in a possible parallel arrangement. Apart from divisors which are equal to 2, also divisors having a different value could be implemented, if necessary. An embodiment of a counter means, such as 8-2, embodied as a 3-counter is shown in figure 6, the 3-counter being built up from easy to integrate 2-counters 26 and 27 having reset inputs

R jointly connected to an output 28 of a gate means formed as an AND-port 29. An output 30 of the counter 26, and an input 31 of the counter 27 are jointly connected to a first input 32 of the AND-port 29, whose second input 33 is connected to output 34 of the counter 27 for outputting a signal whose frequency is divided by 3 relative to the signal on input 35 of the counter 26.

5



**CLAIMS:**

1. A frequency-conversion circuit comprising a multistage frequency-converting means and an oscillator output coupled to at least one oscillator input of the multistage frequency-converting means, characterised in that the frequency-conversion circuit comprises a frequency divider means coupled between the oscillator output and at least one  
5 further oscillator input of the multistage frequency-converting means.
2. The frequency-conversion circuit according to claim 1, characterised in that the multistage frequency-converting means is a two stage frequency-converting means.
3. The frequency-conversion circuit according to claim 1 or 2, characterised in that at least one stage of the multistage frequency-converting means is a quadrature paths  
10 multistage frequency-converting means.
4. The frequency-conversion circuit according to claim 3, characterised in that the quadrature path multistage frequency-converting means has an I-path coupled through an I-path oscillator input to the oscillator output and a Q-path having a Q-path oscillator input, and that the multistage frequency-converting means comprises at least one 90° phase  
15 shifter coupled between the I-path oscillator input and the Q-path oscillator input.
5. The frequency-conversion circuit according to claims 1, 2, 3, or 4, characterised in that the frequency divider means is included in a phase-locked loop.
6. The frequency-conversion circuit according to claim 5, characterised in that the phase-locked loop comprises the oscillator in the form of a local voltage-controlled  
20 oscillator having a control input and an oscillator output coupled to the frequency divider means, and a phase discriminator having a reference frequency input, an input coupled to the frequency divider means and an output coupled to the control input of the voltage-controlled oscillator.
7. The frequency-conversion circuit according to one of the claims 1-6, characterised in that the frequency divider means comprises a counter means.  
25
8. The frequency conversion circuit according to claim 7, characterised in that the counter means comprises a series arrangement and/or parallel arrangement of counters.
9. The frequency-conversion circuit according to claim 7 or 8, characterised

in that the counter means comprises at least a 2-counter.

10. The frequency-conversion circuit according to claim 9, characterised in that the counter means comprises two 2-counters.

11. The frequency-conversion circuit according to claim 10, characterised in  
5 that the frequency-division means comprises gate means connected with the two binar counters in such a manner that a frequency divided by  $n$  means is implemented,  $n$  being an integer.

12. The frequency-conversion circuit according to claim 11, characterised in that  $n$  is 2 or 3.

10 13. A telecommunication system provided with a frequency-conversion circuit comprising a multistage frequency-converting means and an oscillator output coupled to at least one oscillator input of the multistage frequency-converting means, characterised in that the frequency-conversion circuit comprises a frequency divider means coupled between the oscillator output and at least one further oscillator input of the multistage frequency-  
15 converting means.

14. The telecommunication system according to claim 13, characterised in that the telecommunication system is a transmission system, such as a radio transmission system, a cordless or cellular telephone system or the like, an audio- or video system, a control system, a telemetry system, a local area network, a wide area network etcetera.

20 15. A receiver provided with a frequency-conversion circuit according to one of the claims 1-12, the frequency-conversion circuit comprising a multistage frequency-converting means and an oscillator output coupled to at least one oscillator input of the multistage frequency-converting means, characterised in that the frequency conversion circuit comprises a frequency divider means coupled between the oscillator output and at least one  
25 further oscillator input of the multistage frequency-converting means.

16. A transmitter provided with a frequency-conversion circuit according to one of the claims 1-12, the frequency-conversion circuit comprising a multistage frequency converting means and an oscillator output coupled to at least one oscillator input of the multistage frequency-converting means, characterised in that the frequency-conversion circuit  
30 comprises a frequency divider means coupled between the oscillator output and at least one further oscillator input of the multistage frequency converting means.

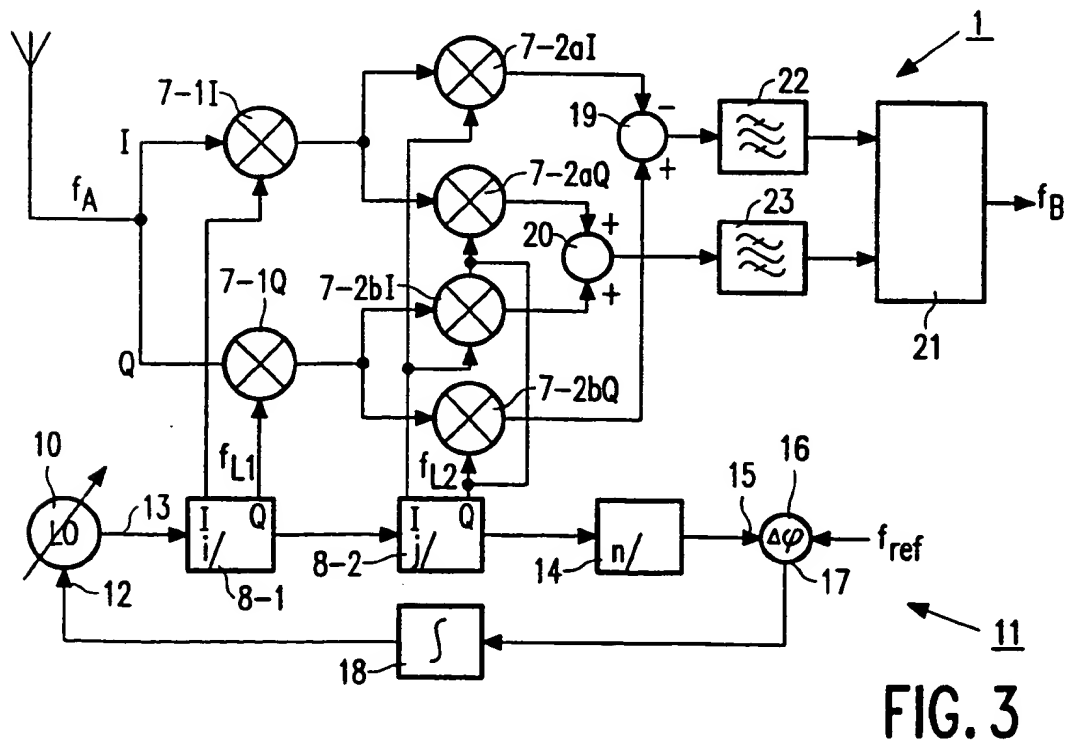
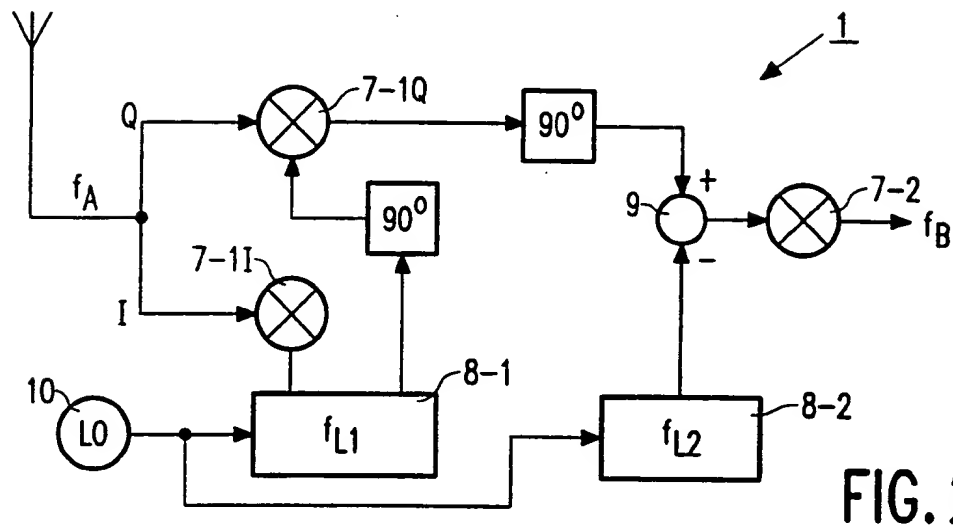
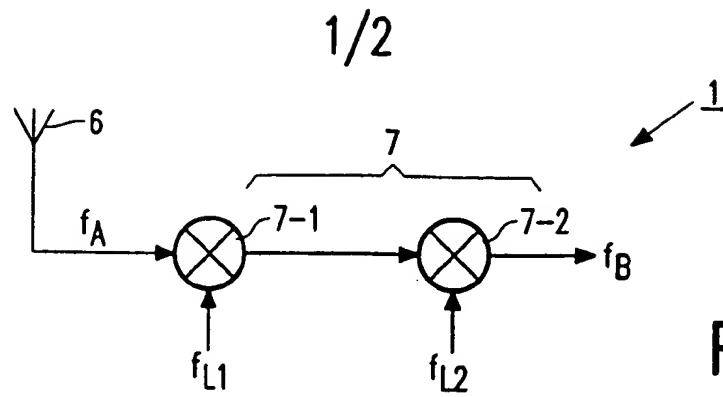
17. A transceiver provided with a frequency-conversion circuit according to one of the claims 1-12, the frequency conversion circuit comprising a multistage frequency-converting means and an oscillator output coupled to at least one oscillator input of the

multistage frequency converting means, characterised in that the frequency-conversion circuit comprises a frequency divider means coupled between the oscillator output and at least one further oscillator input of the multistage frequency converting means.

18. A integrated circuit provided with a frequency-conversion circuit

5 according to one of the claims 1-12, the frequency-conversion circuit comprising a multistage frequency-converting means and an oscillator output coupled to at least one oscillator input of the multistage frequency-converting means, characterised in that the frequency-conversion circuit comprises a frequency divider means coupled between the oscillator output and at least one further oscillator input of the multistage frequency-converting means.

10 19. A telephone device provided with a frequency-conversion circuit according to one of the claims 1-12, the frequency-conversion circuit comprising a multistage frequency-converting means and an oscillator output coupled to at least one oscillator input of the multistage frequency-converting means, characterised in that the frequency-conversion circuit comprises a frequency divider means coupled between the oscillator output and at  
15 least one further oscillator input of the multistage frequency-converting means.



2/2

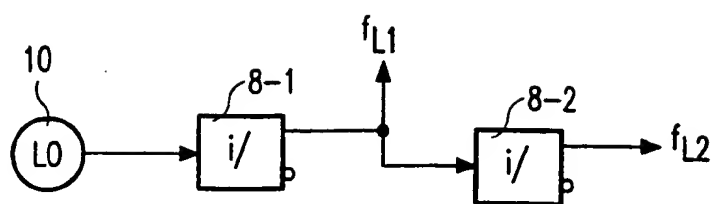


FIG. 4

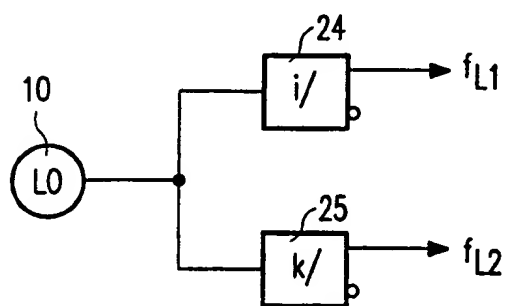


FIG. 5

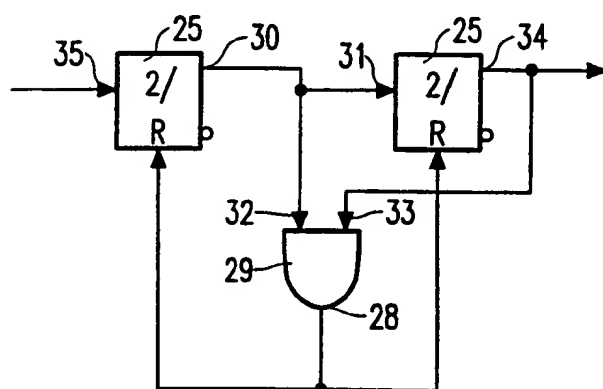


FIG. 6

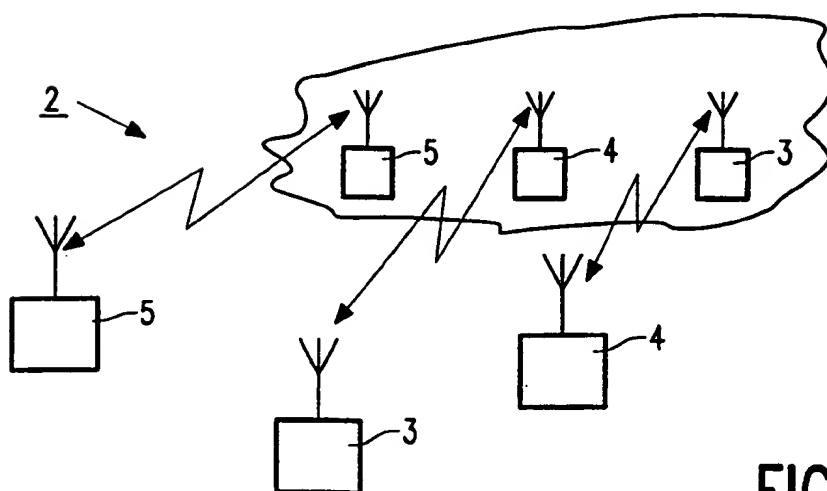


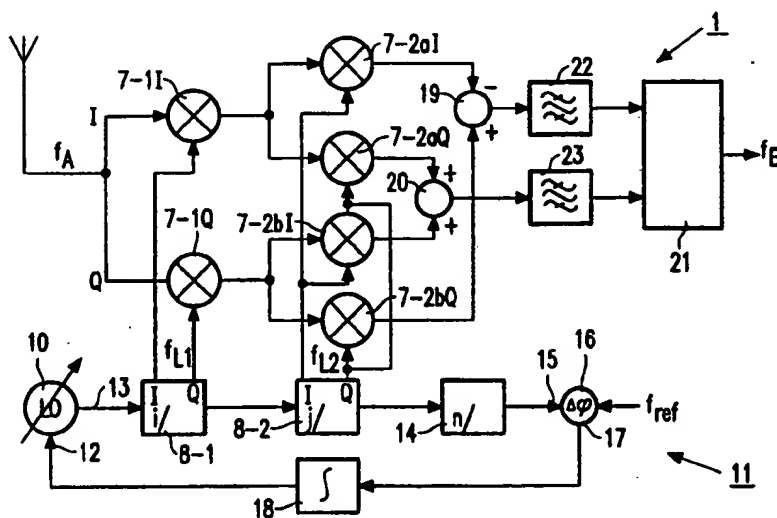
FIG. 7



## INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

<b>(51) International Patent Classification <sup>6</sup> :</b> <b>H03L 7/08, H04B 1/18, 1/40, H03D 7/16</b>	<b>A3</b>	<b>(11) International Publication Number:</b> <b>WO 98/40968</b> <b>(43) International Publication Date:</b> 17 September 1998 (17.09.98)
<b>(21) International Application Number:</b> PCT/IB98/00238 <b>(22) International Filing Date:</b> 27 February 1998 (27.02.98)  <b>(30) Priority Data:</b> 97200739.7 12 March 1997 (12.03.97) EP <b>(34) Countries for which the regional or international application was filed:</b> NL et al.  <b>(71) Applicant:</b> KONINKLIJKE PHILIPS ELECTRONICS N.V. [NL/NL]; Groenewoudseweg 1, NL-5621 BA Eindhoven (NL). <b>(71) Applicant (for SE only):</b> PHILIPS NORDEN AB [SE/SE]; Kottbygatan 7, Kista, S-164 85 Stockholm (SE). <b>(72) Inventor:</b> BALTUS, Petrus, Gerardus; Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL). <b>(74) Agent:</b> MAK, Theodorus, N.; Internationaal Octrooibureau B.V., P.O. Box 220, NL-5600 AE Eindhoven (NL).		<b>(81) Designated States:</b> JP, European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).  <b>Published</b> <i>With international search report.</i>  <b>(88) Date of publication of the international search report:</b> 18 February 1999 (18.02.99)

(54) Title: A FREQUENCY CONVERSION CIRCUIT



## (57) Abstract

In a frequency-conversion circuit having a multistage frequency-converting means, at least two stages are coupled through divider means to one and the same voltage-controlled oscillator. Inputs of the multistage frequency-converting means are coupled to one another in a phase error-free manner by frequency divider means embodied as easy-to-implement counters. By virtue thereof, one phase locked loop including such a voltage-controlled oscillator can be dispensed with, thus saving surface area, components on a chip and reducing costs and weight, which is particularly important in connection with the application of the frequency-conversion circuit in mobile communication equipment.

**FOR THE PURPOSES OF INFORMATION ONLY**

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AL	Albania	ES	Spain	LS	Lesotho	SI	Slovenia
AM	Armenia	FI	Finland	LT	Lithuania	SK	Slovakia
AT	Austria	FR	France	LU	Luxembourg	SN	Senegal
AU	Australia	GA	Gabon	LV	Latvia	SZ	Swaziland
AZ	Azerbaijan	GB	United Kingdom	MC	Monaco	TD	Chad
BA	Bosnia and Herzegovina	GE	Georgia	MD	Republic of Moldova	TG	Togo
BB	Barbados	GH	Ghana	MG	Madagascar	TJ	Tajikistan
BE	Belgium	GN	Guinea	MK	The former Yugoslav Republic of Macedonia	TM	Turkmenistan
BF	Burkina Faso	GR	Greece			TR	Turkey
BG	Bulgaria	HU	Hungary	ML	Mali	TT	Trinidad and Tobago
BJ	Benin	IE	Ireland	MN	Mongolia	UA	Ukraine
BR	Brazil	IL	Israel	MR	Mauritania	UG	Uganda
BY	Belarus	IS	Iceland	MW	Malawi	US	United States of America
CA	Canada	IT	Italy	MX	Mexico	UZ	Uzbekistan
CF	Central African Republic	JP	Japan	NE	Niger	VN	Viet Nam
CG	Congo	KE	Kenya	NL	Netherlands	YU	Yugoslavia
CH	Switzerland	KG	Kyrgyzstan	NO	Norway	ZW	Zimbabwe
CI	Côte d'Ivoire	KP	Democratic People's Republic of Korea	NZ	New Zealand		
CM	Cameroon			PL	Poland		
CN	China	KR	Republic of Korea	PT	Portugal		
CU	Cuba	KZ	Kazakstan	RO	Romania		
CZ	Czech Republic	LC	Saint Lucia	RU	Russian Federation		
DE	Germany	LI	Liechtenstein	SD	Sudan		
DK	Denmark	LK	Sri Lanka	SE	Sweden		
EE	Estonia	LR	Liberia	SG	Singapore		

## INTERNATIONAL SEARCH REPORT

International application No.

PCT/IB 98/00238

## A. CLASSIFICATION OF SUBJECT MATTER

IPC6: H03L 7/08, H04B 1/18, H04B 1/40, H03D 7/16

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC6: H03L, H04B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

SE,DK,FI,NO classes as above

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EDOC, WPIL, JAPIO

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	Patent Abstracts of Japan, abstract of JP 63-175507 A (TOSHIBA CORP), 19 July 1988 (19.07.88)	1,2,7,13,14
Y	--	3,4,15-19
Y	DE 3726181 A1 (AUTOPHON AG), 10 March 1988 (10.03.88), figure 1, abstract	3,4,15-19
A	-- -----	1,2

☐ Further documents are listed in the continuation of Box C.☒ See patent family annex.

\* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance: the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance: the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&amp;" document member of the same patent family

Date of the actual completion of the international search

10 December 1998

Date of mailing of the international search report

15 -12- 1998

Name and mailing address of the ISA:

Swedish Patent Office

Box 5055, S-102 42 STOCKHOLM

Facsimile No. +46 8 666 02 86

Authorized officer

Bo Gustavsson

Telephone No. +46 8 782 25 00



### Information on patent family members

International application No.

— 1 —

Form PCT/ISA/210 (patent family annex) (July 1992)